K210
Datasheet

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About This Guide

This document provides the specifications of Kendryte family of chips.

Revision History

Date	Ver.	Revision History
2018-09-01	V0.1.0	Initial release
2018-09-13	V0.1.1	Fixing the wrong description in SPI and GPIO
2018-09-14	V0.1.2	Correction of errors in Chapter 1
2018-09-17	V0.1.3	Correction of pin description error in Chapter 2
2018-09-18	V0.1.4	Adding Kendryte system architecture diagram
2018-09-19	V0.1.5	Fixed an error description of the timer

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Contents

Chapter 1

Overview

The Kendryte K210 is a system-on-chip (SoC) that integrates machine vision and machine hearing. Using TSMC' s ultra-low-power 28-nm advanced process with dual-core 64-bit processors for better power efficiency, stability and reliability. The SoC strives for " zero threshold" development and to be deployable in the user' s products in the shortest possible time, giving the product artificial intelligence.

Kendryte K210 is intended for the AI and IoT markets, but is also a high-performance MCU.

Kendryte in Chinese means researching intelligence. The main application field of this chip is in the field of Internet of Things. The chip provides AI solutions to add intelligence to this.

- Machine Vision
- Machine Hearing
- Better low power vision processing speed and accuracy
- KPU high performance Convolutional Neural Network (CNN) hardware accelerator
- Advanced TSMC 28nm process, temperature range -40°C to 125°C
- Firmware encryption support
- Unique programmable IO array maximises design flexibility
- Low voltage, reduced power consumption compared to other systems with the same processing power
- 3.3V/1.8V dual voltage IO support eliminates need for level shifters

1.1 AI solution

1.1.1 Machine Vision

With machine vision capabilities, the Kendryte K210 is a zero-threshold embedded machine vision solution. It can perform convolutional neural network calculations with low power consumption.

Capabilities:

- Object Detection
- Image Classification
- Face Detection and Recognition
- Obtaining size and coordinates of target in real time
- Obtaining type of detected target in real time

1.1.2 Machine Hearing

The Kendryte K210 has machine hearing capabilities. The chip comes with a high-performance microphone array audio processor for real-time source orientation and beamforming.

Capabilities:

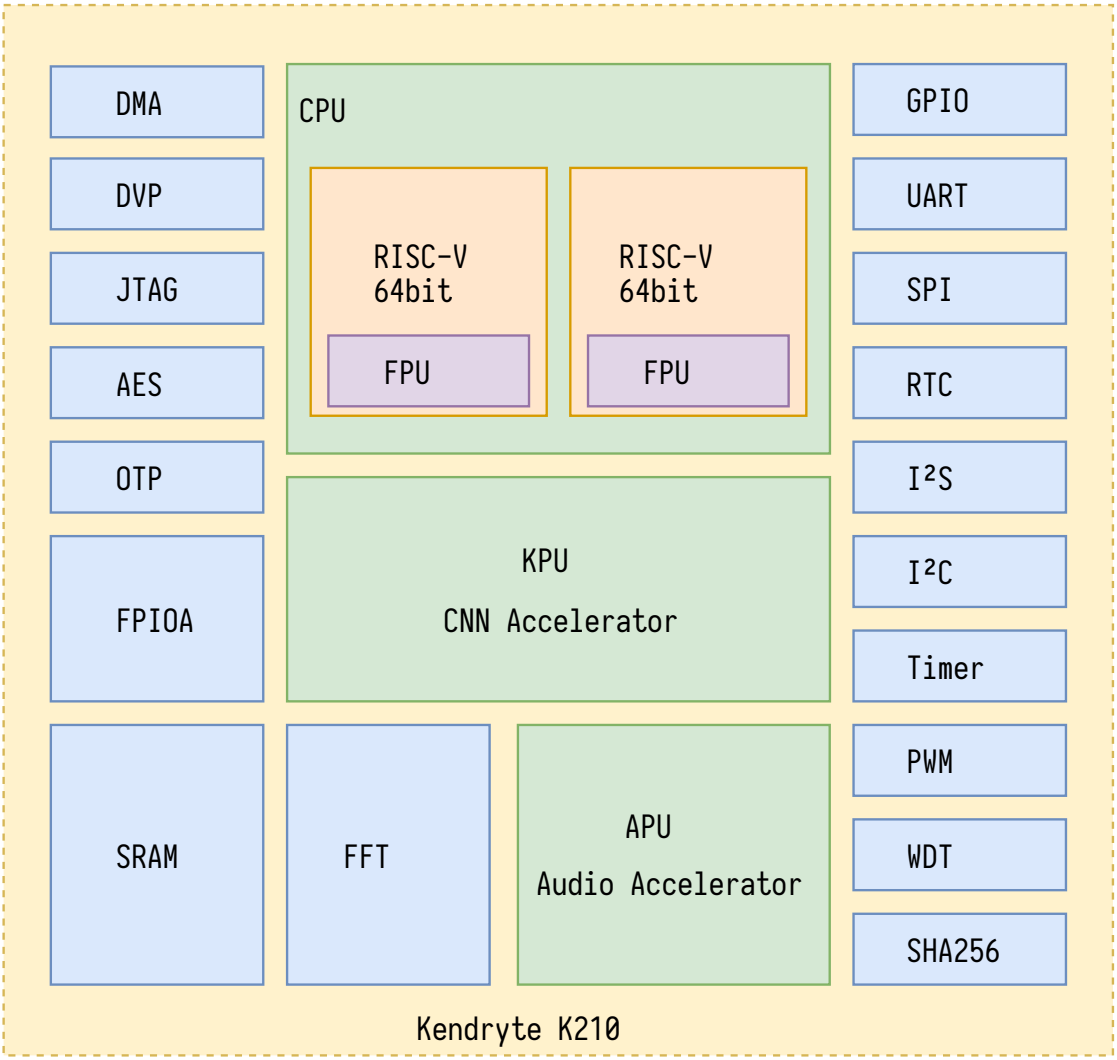
- Sound source orientation detection
- Sound Field Imaging
- Beamforming
- Voice Wake-Up
- Speech Recognition

1.1.3 Hybrid Audio/Vision Solution

The Kendryte K210 combines machine vision and machine hearing to provide even more powerful features. In the application, both the sound source localization and the sound field imaging can be used to assist the machine vision to track the target, and the general target detection can obtain the target' s orientation and then assist the machine to perform the beamforming of the source. Additionally, the direction of the person can be obtained by the image transmitted from the camera, so that the microphone array is directed to the person by beamforming. At the same

time, the direction of speech can be determined according to the microphone array, and the camera is rotated to point to the person.

1.2 Architecture Overview



The K210 includes two 64-bit RISC-V CPU cores, each with a built-in independent FPU. The primary functions of the K210 are machine vision and hearing, which includes the KPU for computing convolutional neural networks and an APU for processing microphone array inputs. The K210 features a Fast Fourier Transform (FFT) Accelerator for high performance complex FFT calculations. As a result, for most machine learning algorithms, the K210 has high-performance processing power.

The K210 embeds AES and SHA256 algorithm accelerators to provide users with basic security features.

The K210 features high-performance, low-power SRAM and powerful DMA for superior data throughput.

K210 has a wide range of peripheral units: DVP, JTAG, OTP, FPIOA, GPIO, UART, SPI, RTC, I2S, I2C, WDT, Timer and PWM, for a large number of application scenarios.

Chapter 2

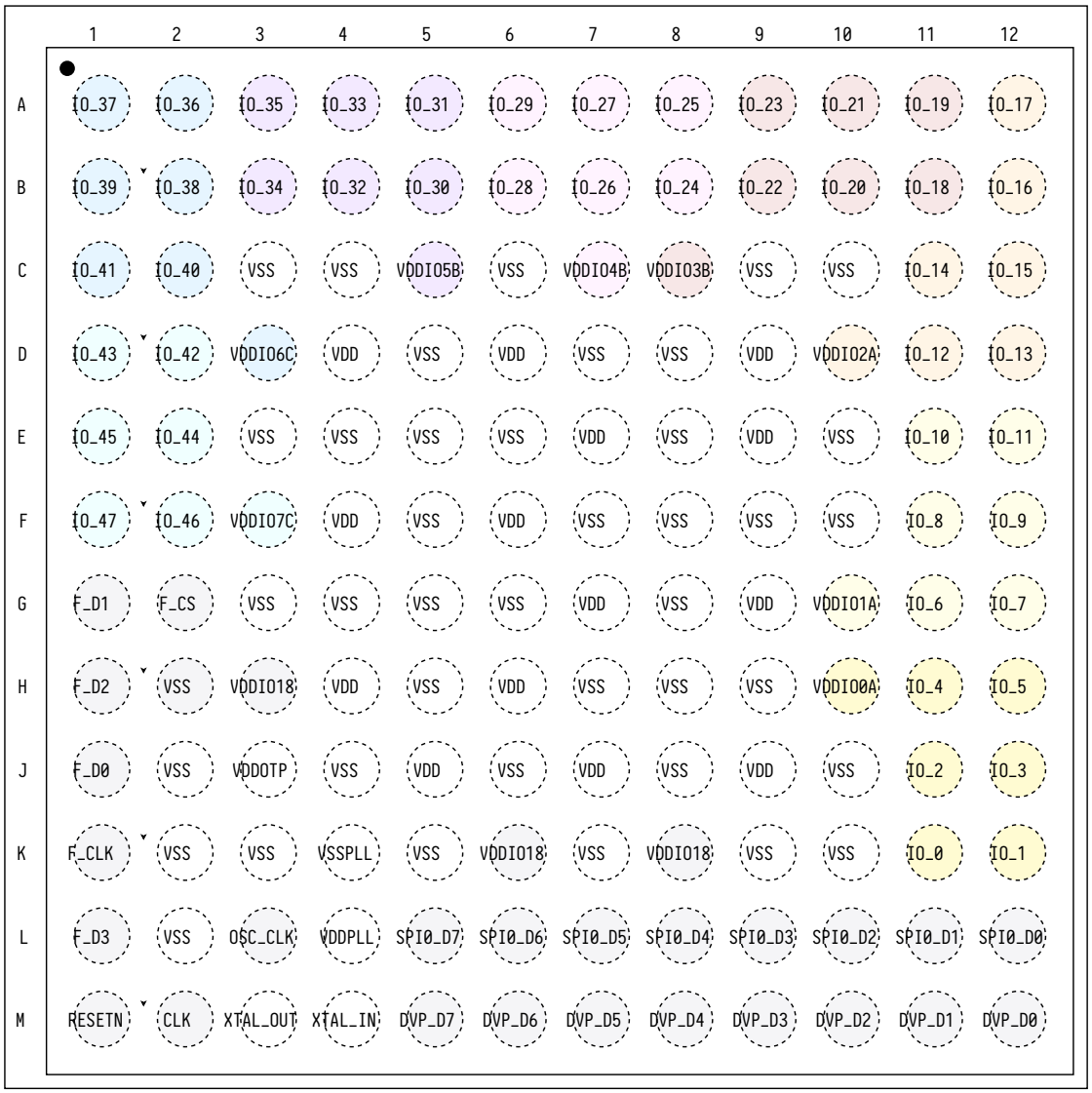
Pin Specifications

The K210 uses a well-designed pin layout to ensure that the signals are on the BGA outer ring to allow PCB designers to fanout and route easily, improve electrical performance and reduce design difficulty.

Since the K210 contains multiple IO signals from the power domain and different power domains may have different voltages, the following will list the power domains used:

Power Group	Power Domain	Voltage (V)	Connected to	Name
A	0	3.3/1.8	Other domains in group	VDDIO0A
A	1	3.3/1.8	Other domains in group	VDDIO1A
A	2	3.3/1.8	Other domains in group	VDDIO2A
B	3	3.3/1.8	Other domains in group	VDDIO3B
B	4	3.3/1.8	Other domains in group	VDDIO4B
B	5	3.3/1.8	Other domains in group	VDDIO5B
C	6	3.3/1.8	Other domains in group	VDDIO6C
C	7	3.3/1.8	Other domains in group	VDDIO7C
LV IO	LV IO	1.8	Independent	VDDIO18
OTP	OTP	1.8	Independent	VDDOTP
PLL	PLL	0.9	Independent	VDDPLL
Core	Core	0.9	Independent	VDD

2.1 Pin Layout



The pin definition of the chip is as shown above (top view, solder balls facing downwards). The chip is packaged in a BGA144, square, with 12 pins on each side. The chip has a width of 8mm, a length of 8mm and a height of 0.953mm.

2.2 Pin Description

Ball	Name	Type	Function	Reset State
A1	IO_37	I/O	Multifunctional IO (FPIOA) (Bank 6, Group C)	GPIOHS21
A2	IO_36	I/O	Multifunctional IO (FPIOA) (Bank 6, Group C)	GPIOHS20
A3	IO_35	I/O	Multifunctional IO (FPIOA) (Bank 5, Group B)	GPIOHS19
A4	IO_33	I/O	Multifunctional IO (FPIOA) (Bank 5, Group B)	GPIOHS17
A5	IO_31	I/O	Multifunctional IO (FPIOA) (Bank 5, Group B)	GPIOHS15
A6	IO_29	I/O	Multifunctional IO (FPIOA) (Bank 4, Group B)	GPIOHS13
A7	IO_27	I/O	Multifunctional IO (FPIOA) (Bank 4, Group B)	GPIOHS11
A8	IO_25	I/O	Multifunctional IO (FPIOA) (Bank 4, Group B)	GPIOHS9
A9	IO_23	I/O	Multifunctional IO (FPIOA) (Bank 3, Group B)	GPIOHS7
A10	IO_21	I/O	Multifunctional IO (FPIOA) (Bank 3, Group B)	GPIOHS5
A11	IO_19	I/O	Multifunctional IO (FPIOA) (Bank 3, Group B)	GPIOHS3
A12	IO_17	I/O	Multifunctional IO (FPIOA) (Bank 2, Group A)	GPIOHS1
B1	IO_39	I/O	Multifunctional IO (FPIOA) (Bank 6, Group C)	GPIOHS23
B2	IO_38	I/O	Multifunctional IO (FPIOA) (Bank 6, Group C)	GPIOHS22
B3	IO_34	I/O	Multifunctional IO (FPIOA) (Bank 5, Group B)	GPIOHS18
B4	IO_32	I/O	Multifunctional IO (FPIOA) (Bank 5, Group B)	GPIOHS16
B5	IO_30	I/O	Multifunctional IO (FPIOA) (Bank 5, Group B)	GPIOHS14
B6	IO_28	I/O	Multifunctional IO (FPIOA) (Bank 4, Group B)	GPIOHS12
B7	IO_26	I/O	Multifunctional IO (FPIOA) (Bank 4, Group B)	GPIOHS10
B8	IO_24	I/O	Multifunctional IO (FPIOA) (Bank 4, Group B)	GPIOHS8
B9	IO_22	I/O	Multifunctional IO (FPIOA) (Bank 3, Group B)	GPIOHS6
B10	IO_20	I/O	Multifunctional IO (FPIOA) (Bank 3, Group B)	GPIOHS4
B11	IO_18	I/O	Multifunctional IO (FPIOA) (Bank 3, Group B)	GPIOHS2
B12	IO_16	I/O	Multifunctional IO (FPIOA) (Bank 2, Group A)	GPIOHS0 (ISP)
C1	IO_41	I/O	Multifunctional IO (FPIOA) (Bank 6, Group C)	GPIOHS25
C2	IO_40	I/O	Multifunctional IO (FPIOA) (Bank 6, Group C)	GPIOHS24
C3	VSS	S	Ground	VSS
C4	VSS	S	Ground	VSS
C5	VDDIO5B	S	3.3V/1.8V supply for FPIOA IO (Bank 5, Group B)	VDDIO33
C6	VSS	S	Ground	VSS
C7	VDDIO4B	S	3.3V/1.8V supply for FPIOA IO (Bank 4, Group B)	VDDIO33
C8	VDDIO3B	S	3.3V/1.8V supply for FPIOA IO (Bank 3, Group B)	VDDIO33
C9	VSS	S	Ground	VSS
C10	VSS	S	Ground	VSS
C11	IO_14	I/O	Multifunctional IO (FPIOA) (Bank 2, Group A)	GPIO6

Ball	Name	Type	Function	Reset State
C12	IO_15	I/O	Multifunctional IO (FPIOA) (Bank 2, Group A)	GPIO7
D1	IO_43	I/O	Multifunctional IO (FPIOA) (Bank 7, Group C)	GPIOHS27
D2	IO_42	I/O	Multifunctional IO (FPIOA) (Bank 7, Group C)	GPIOHS26
D3	VDDIO6C	S	3.3V/1.8V supply for FPIOA IO (Bank 6, Group C)	VDDIO33
D4	VDD	S	0.9V digital core supply	VDD
D5	VSS	S	Ground	VSS
D6	VDD	S	0.9V digital core supply	VDD
D7	VSS	S	Ground	VSS
D8	VSS	S	Ground	VSS
D9	VDD	S	0.9V digital core supply	VDD
D10	VDDIO2A	S	3.3V/1.8V supply for FPIOA IO (Bank 2, Group A)	VDDIO33
D11	IO_12	I/O	Multifunctional IO (FPIOA) (Bank 2, Group A)	GPIO4
D12	IO_13	I/O	Multifunctional IO (FPIOA) (Bank 2, Group A)	GPIO5
E1	IO_45	I/O	Multifunctional IO (FPIOA) (Bank 7, Group C)	GPIOHS29
E2	IO_44	I/O	Multifunctional IO (FPIOA) (Bank 7, Group C)	GPIOHS28
E3	VSS	S	Ground	VSS
E4	VSS	S	Ground	VSS
E5	VSS	S	Ground	VSS
E6	VSS	S	Ground	VSS
E7	VDD	S	0.9V digital core supply	VDD
E8	VSS	S	Ground	VSS
E9	VDD	S	0.9V digital core supply	VDD
E10	VSS	S	Ground	VSS
E11	IO_10	I/O	Multifunctional IO (FPIOA) (Bank 1, Group A)	GPIO2
E12	IO_11	I/O	Multifunctional IO (FPIOA) (Bank 1, Group A)	GPIO3
F1	IO_47	I/O	Multifunctional IO (FPIOA) (Bank 7, Group C)	GPIOHS31
F2	IO_46	I/O	Multifunctional IO (FPIOA) (Bank 7, Group C)	GPIOHS30
F3	VDDIO7C	S	3.3V/1.8V supply for FPIOA IO (Bank 7, Group C)	VDDIO33
F4	VDD	S	0.9V digital core supply	VDD
F5	VSS	S	Ground	VSS
F6	VDD	S	0.9V digital core supply	VDD
F7	VSS	S	Ground	VSS
F8	VSS	S	Ground	VSS
F9	VSS	S	Ground	VSS
F10	VSS	S	Ground	VSS

Ball	Name	Type	Function	Reset State
F11	IO_8	I/O	Multifunctional IO (FPIOA) (Bank 1, Group A)	GPIO0
F12	IO_9	I/O	Multifunctional IO (FPIOA) (Bank 1, Group A)	GPIO1
G1	F_D1	I/O	Dedicated SPI GPIO (1.8V only)	F_D1
G2	F_CS	O	Dedicated SPI GPIO (1.8V only)	F_CS
G3	VSS	S	Ground	VSS
G4	VSS	S	Ground	VSS
G5	VSS	S	Ground	VSS
G6	VSS	S	Ground	VSS
G7	VDD	S	0.9V digital core supply	VDD
G8	VSS	S	Ground	VSS
G9	VDD	S	0.9V digital core supply	VDD
G10	VDDIO1A	S	3.3V/1.8V supply for FPIOA IO (Bank 1, Group A)	VDDIO33
G11	IO_6	I/O	Multifunctional IO (FPIOA) (Bank 1, Group A)	(FLOAT*)
G12	IO_7	I/O	Multifunctional IO (FPIOA) (Bank 1, Group A)	(FLOAT*)
H1	F_D2	I/O	Dedicated SPI GPIO (1.8V only)	F_D2
H2	VSS	S	Ground	VSS
H3	VDDIO18	S	1.8V supply for low voltage IO	VDDIO18
H4	VDD	S	0.9V digital core supply	VDD
H5	VSS	S	Ground	VSS
H6	VDD	S	0.9V digital core supply	VDD
H7	VSS	S	Ground	VSS
H8	VSS	S	Ground	VSS
H9	VSS	S	Ground	VSS
H10	VDDIO0A	S	3.3V/1.8V supply for FPIOA IO(Bank 0, Group A)	VDDIO33
H11	IO_4	I/O	Multifunctional IO (FPIOA) (Bank 0, Group A)	UARTHS_RX (ISP)
H12	IO_5	I/O	Multifunctional IO (FPIOA) (Bank 0, Group A)	UARTHS_TX (ISP)
J1	F_D0	I/O	Dedicated SPI GPIO (1.8V only)	F_D0
J2	VSS	S	Ground	VSS
J3	VDDOTP	S	1.8V OTP supply	VDDOTP
J4	VSS	S	Ground	VSS
J5	VDD	S	0.9V digital core supply	VDD
J6	VSS	S	Ground	VSS
J7	VDD	S	0.9V digital core supply	VDD
J8	VSS	S	Ground	VSS
J9	VDD	S	0.9V digital core supply	VDD

Ball	Name	Type	Function	Reset State
J10	VSS	S	Ground	VSS
J11	IO_2	I/O	Multifunctional IO (FPIOA) (Bank 0, Group A)	JTAG_TMS
J12	IO_3	I/O	Multifunctional IO (FPIOA) (Bank 0, Group A)	JTAG_TDO
K1	F_CLK	O	Dedicated SPI GPIO (1.8V only)	F_CLK
K2	VSS	S	Ground	VSS
K3	VSS	S	Ground	VSS
K4	VSSPLL	S	PLL analog ground, noise sensitive	VSSPLL
K5	VSS	S	Ground	VSS
K6	VDDIO18	S	1.8V supply for low voltage IO	VDDIO18
K7	VSS	S	Ground	VSS
K8	VDDIO18	S	1.8V supply for low voltage IO	VDDIO18
K9	VSS	S	Ground	VSS
K10	VSS	S	Ground	VSS
K11	IO_0	I/O	Multifunctional IO (FPIOA) (Bank 0, Group A)	JTAG_TCLK
K12	IO_1	I/O	Multifunctional IO (FPIOA) (Bank 0, Group A)	JTAG_TDI
L1	F_D3	I/O	Dedicated SPI GPIO (1.8V only)	F_D3
L2	VSS	S	Ground	VSS
L3	OSC_CLK	O	Active oscillator output	OSC_CLK
L4	VDDPLL	S	0.9V PLL Analog Supply	VDDPLL
L5	SPI0_D7	O	Dedicated SPI0 D7 output	(FLOAT*)
L6	SPI0_D6	O	Dedicated SPI0 D6 output	(FLOAT*)
L7	SPI0_D5	O	Dedicated SPI0 D5 output	(FLOAT*)
L8	SPI0_D4	O	Dedicated SPI0 D4 output	(FLOAT*)
L9	SPI0_D3	O	Dedicated SPI0 D3 output	(FLOAT*)
L10	SPI0_D2	O	Dedicated SPI0 D2 output	(FLOAT*)
L11	SPI0_D1	O	Dedicated SPI0 D1 output	(FLOAT*)
L12	SPI0_D0	O	Dedicated SPI0 D0 output	(FLOAT*)
M1	RESET	I	System Reset, active low	RESET
M2	CLK	I	System Clock input	CLK
M3	XTAL_OUT	O	Passive Crystal Oscillator output (crystal only)	XTAL_OUT
M4	XTAL_IN	I	Passive Crystal Oscillator input (crystal only)	XTAL_IN
M5	DVP_D7	I	Dedicated DVP D7 input	(FLOAT*)
M6	DVP_D6	I	Dedicated DVP D6 input	(FLOAT*)
M7	DVP_D5	I	Dedicated DVP D5 input	(FLOAT*)
M8	DVP_D4	I	Dedicated DVP D4 input	(FLOAT*)

Ball	Name	Type	Function	Reset State
M9	DVP_D3	I	Dedicated DVP D3 input	(FLOAT*)
M10	DVP_D2	I	Dedicated DVP D2 input	(FLOAT*)
M11	DVP_D1	I	Dedicated DVP D1 input	(FLOAT*)
M12	DVP_D0	I	Dedicated DVP D0 input	(FLOAT*)

Key:

Code	Meaning
(FLOAT*)	no default function
I	input
O	output
I/O	input/output
S	power supply

2.3 Power Supplies

Supply	Name	Voltage (V)	Max Current (mA)
I/O 3.3V/1.8V	VDDIO0A	3.3/1.8V[*1]	200
I/O 3.3V/1.8V	VDDIO1A	3.3/1.8V	200
I/O 3.3V/1.8V	VDDIO2A	3.3/1.8V	200
I/O 3.3V/1.8V	VDDIO3B	3.3/1.8V	200
I/O 3.3V/1.8V	VDDIO4B	3.3/1.8V	200
I/O 3.3V/1.8V	VDDIO5B	3.3/1.8V	200
I/O 3.3V/1.8V	VDDIO6C	3.3/1.8V	200
I/O 3.3V/1.8V	VDDIO7C	3.3/1.8V	200
I/O 1.8V	VDDIO18	1.8	200
OTP 1.8V	VDDOTP	1.8	50
Core 0.9V	VDD	0.9	2000
SoC	VSS	0	-
PLL 0.9V	VDDPLL	0.9	15

[*1] Note : There are no connections between the three IO power supply groups A, B and C; the voltage need not be the same between different groups. However the IO power supplies within each group are interconnected and must all be at the same voltage.

Supply	Name	Voltage (V)	Max Current (mA)
PLL	VSSPLL	0	-

2.4 Reset Circuitry

It is recommended to use a 1.8V output MCU power supply monitor IC in order to ensure a stable reset under power-on, power-down and under-voltage conditions.

2.5 Special Pins

IO_16 is used for boot mode selection. During power-on reset, pull high to boot from FLASH and pull low to enter ISP mode. After reset, IO_0, IO_1, IO_2, and IO_3 are JTAG pins. IO_4 and IO_5 are ISP pins.

Chapter 3

Functional Description

3.1 CPU

The chip contains a high-performance, low power RISC-V ISA-based dual core 64-bit CPU with the following features:

Feature		Details
Core Count	2 cores	Dual-core processor, each core with independent FPU
Bit Width	64 bit	64-bit CPU bit width for high-performance algorithm calculations with sufficient computational bandwidth
Frequency	400MHz	Frequency adjustable, can be changed by adjusting PLL VCO and frequency dividers
ISA extensions	IMAFDC	Based on RISC-V 64-bit IMAFDC (RV64GC), suitable for general tasks
FPU	Double Precision	With multiply, divide and square root operations; supports single-precision and double-precision floating-point calculations
Platform Interrupts	PLIC	Supports advanced interrupt management; with 64 external interrupt sources routeable to 2 cores
Local Interrupts	CLINT	With built-in CPU timer interrupt and cross-core interrupt
I-Cache	32KiB × 2	Cores 0 and 1 each have a 32 KiB instruction cache to improve dual-core instruction read performance

Feature		Details
D-Cache	32KiB × 2	Cores 0 and 1 each have a 32 KiB data cache to improve dual-core data read performance
On-Chip SRAM	8MiB	8MiB of on-chip SRAM in total, see SRAM chapter for details

3.1.1 CPU ISA Features

- Powerful dual-core 64-bit open architecture-based processor with rich community resources
- I extension: Base Integer Instruction Set
- M extension: integer multiplication and division; hardware acceleration to achieve high performance integer multiplication and division
- A extension: atomic operations, hardware implementation of the atomic operations required by operating systems
- C extension: compressed instructions, which can achieve higher code density and operation efficiency
- Support for different privilege levels to improve safety

3.1.2 FPU Specifications

- IEEE754-2008 compliant high-performance pipelined FPU
- Core 0 and Core 1 each have a separate FPU, and both cores are capable of high performance hardware floating point calculations
- F extension: single-precision floating point instructions
- D extension: double-precision floating point instructions
- Hardware single-precision and double-precision division
- Hardware single-precision and double-precision square roots

3.1.3 Advanced Interrupt Management Capability

The PLIC controller of the RISC-V CPU supports flexible advanced interrupt management. It can be configured with 64 external interrupt sources in 7 priority levels. Both cores can be configured independently:

- Interrupt management and interrupt routing can be controlled independently for

both cores
- Support for software interrupts, and each core can trigger cross-core interrupts
- Built-in CPU timer interrupt, both cores are freely configurable
- Advanced external interrupt management, supporting 64 external interrupt sources, each interrupt source can be configured with 7 priority levels

3.1.4 Debugging Support

- Support performance monitoring instructions to count instruction execution cycles
- High-speed UART and JTAG interface for debugging
- Support DEBUG mode and hardware breakpoints

3.2 Neural Network Processor (KPU)

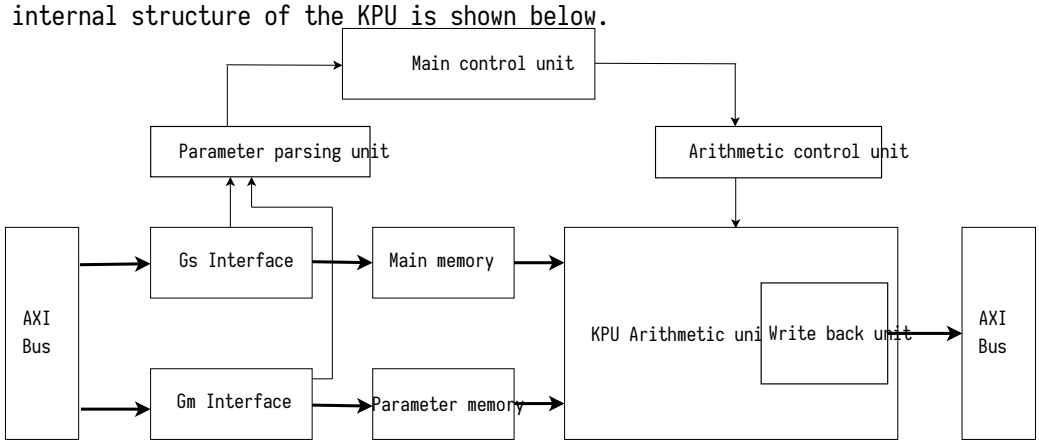
KPU is a general-purpose neural network processor with built-in convolution, batch normalization, activation, and pooling operations. It can detect faces or objects in real time. The specific characteristics are as follows:

- Supports the fixed-point model that the mainstream training framework trains according to specific restriction rules
- There is no direct limit on the number of network layers, and each layer of convolutional neural network parameters can be configured separately, including the number of input and output channels, and the input and output line width and column height
- Support for 1x1 and 3x3 convolution kernels
- Support for any form of activation function
- The maximum supported neural network parameter size for real-time work is 5MiB to 5.9MiB
- The maximum supported network parameter size when working in non-real time is (flash size - software size)

Mode	Maximum fixed point model size (MiB)	Maximum pre-quantisation floating point model size (MiB)
Realtime (≥ 30fps)	5.9	11.8

Mode	Maximum fixed point model size (MiB)	Maximum pre-quantisation floating point model size (MiB)
Non-realtime (< 10fps)*1	Flash Capacity*2	Flash Capacity

The internal structure of the KPU is shown below.



3.3 Audio Processor (APU)

The APU pre-processing module is responsible for the pre-processing of voice direction and voice data output. The functional characteristics of the APU pre-processing module are:

- Up to 8 channels of audio input data, ie 4 stereo channels
- Simultaneous scanning pre-processing and beamforming for sound sources in up to 16 directions
- Supports one active voice stream output
- 16-bit wide internal audio signal processing
- Support for 12-bit, 16-bit, 24-bit, and 32-bit input data widths
- Multi-channel direct raw signal output
- Up to 192kHz sample rate
- Built-in FFT unit supports 512-point FFT of audio data
- Uses system DMAC to store output data in system memory

*1 Non-real-time applications generally include audio applications, as such applications generally do not require neural network output within 33 ms.

*2 Flash size support : SPI NOR Flash (8MiB, 16MiB, 32MiB), SPI NAND Flash (64MiB, 128MiB, 256MiB)

3.4 Static Random-Access Memory (SRAM)

The SRAM is split into two parts, 6MiB of on-chip general-purpose SRAM memory and 2MiB of on-chip AI SRAM memory, for a total of 8MiB. The AI SRAM memory is memory allocated for the KPU. They are distributed in a contiguous address space, available both through the normal cached interface of the CPU, but also directly through the non-cached interface.

SRAM address map :

Region	Access	Start Address	End Address	Size
General-purpose SRAM	CPU cached	0x80000000	0x805FFFFF	0x600000
AI SRAM	CPU cached	0x80600000	0x807FFFFF	0x200000
General-purpose SRAM	CPU non-cached	0x40000000	0x405FFFFF	0x600000
AI SRAM	CPU non-cached	0x40600000	0x407FFFFF	0x200000

3.4.1 General Purpose SRAM

The general purpose SRAM memory is accessible at all times during normal operation of the chip. The memory is divided into two banks, MEM0 and MEM1, and the DMA controller can operate in both banks at the same time.

** General-purpose SRAM address map : **

Region	Access	Start Address	End Address	Size
MEM0	CPU cached	0x80000000	0x803FFFFF	0x400000
MEM1	CPU cached	0x80400000	0x805FFFFF	0x200000
MEM0	CPU non-cached	0x40000000	0x403FFFFF	0x400000
MEM1	CPU non-cached	0x40400000	0x405FFFFF	0x200000

3.4.2 AI SRAM

The AI SRAM memory is only accessible if the following conditions are met:

- PLL1 enabled and clock system configuration is correct
- KPU not performing neural network calculations

AI SRAM address map :

Region	Access	Start Address	End Address	Size
AI SRAM	CPU cached	0x80600000	0x807FFFFF	0x200000
AI SRAM	CPU non-cached	0x40600000	0x407FFFFF	0x200000

3.5 System Controller (SYSCTL)

Controls chip clocking and reset and contains the following general system control registers:

- PLL frequency
- Clock selection
- Peripheral clock division ratios
- Clock enables
- Module resets
- DMA handshake signal selection

3.6 Field Programmable IO Array (FPIOA/IOMUX)

FPIOA allows users to map 255 internal functions to 48 free IOs on the chip:

- Programmable IO function selection
- 8 drive strength options for outputs
- Selectable internal pull-up resistors
- Selectable internal pull-down resistors
- Schmitt trigger option for inputs
- Slew rate control for outputs
- Selectable internal input level

3.7 One-Time Programmable Memory (OTP)

OTP is a one-time programmable memory unit. The specifications are as follows:

- Large 128Kbit storage capacity
- Internally divided into multiple BLOCKs with different capacity; each with a separate write protection bit

- Dead bit repair support
- 64 REGISTER_ENABLE flag bits, can be used as a switch to control the behaviour of some SoC hardware circuits
- Can store 128-bit AES encryption and decryption KEY, hardware write-only trusted storage area

3.8 AES Accelerator

The AES accelerator is a module for encryption and decryption. The specifications are as follows:

- ECB, CBC, and GCM encryption methods
- 128-bit, 192-bit or 256-bit key
- Key can be configured by software and protected by hardware circuit
- DMA transfer support

3.9 Digital Video Port (DVP)

The DVP is a camera interface module with the following features:

- Supports cameras with a DVP interface
- Supports camera configuration using SCCB protocol
- Maximum frame size 640x480
- Supports YUV422 and RGB565 format image input
- Can output images to both KPU and display
  - Output format to KPU: RGB888 or the Y component of YUV422 input
  - Output format to display: RGB565
- Interrupt can be sent to CPU for start-of-frame or completion of frame image transmission

3.10 FFT Accelerator

The FFT accelerator is a hardware implementation of the Fast Fourier Transform (FFT).

- 64-point, 128-point, 256-point or 512-point length
- FFT and IFFT operation modes

- 32-bit or 64-bit input data width
- Supports pure-real, pure-imaginary or complex input data
- DMA transfer support

3.11 SHA256 Accelerator

The SHA256 accelerator is a computational unit used to calculate SHA-256:

- SHA-256 calculation
- DMA transfer support for input data

3.12 Universal Asynchronous Transceiver (UART)

3.12.1 High Speed UART :

High speed UART UARTHS(UART0)

- Baud rate up to 5Mbps
- 8-byte transmit and receive FIFO
- Programmable THRE interrupt
- Does not support hardware flow control or other modem control signals, or synchronous serial data protocols

3.12.2 General Purpose UART :

UART1, UART2 and UART3 are general purpose UARTs and support asynchronous communication (RS232/RS485/IRDA), baud rate up to 5Mbps, hardware flow control using CTS/RTS or (XON/XOFF). All three interfaces can be accessed by DMA or directly by the CPU.

- 8-byte transmit and receive FIFO
- Asynchronous clock support
  - In order to cope with the CPU' s baud rate requirement for data synchronization, the UART can configure the data clock separately for transmit and receive. The full-duplex mode can ensure the synchronization of data in the two clock domains.
- RS485 interface support
  - The UART can be configured by software into RS485 mode. The default is

RS232 mode

- Programmable THRE interrupt
  - Use THRE interrupt mode to improve serial port performance. After the THRE mode and FIFO mode are selected, the THRE interrupt is triggered if there is less than the threshold in the FIFO.

3.13 Watchdog Timer (WDT)

The WDT is a slave peripheral to the APB and is part of the ” common hardware component design.” It has two WDTs: WDT0, WDT1. The watchdog timer contains the following modules:

- An APB slave interface
- A register module that synchronizes the current counter
- An interrupt/system reset module and logic control circuit with down counter
- A synchronous clock domain to support asynchronous clock synchronization

The watchdog timer supports the following settings:

- APB bus width can be configured to 8, 16, and 32 bits
- The clock counter is decremented from a certain set value to 0 to indicate timeout
- Optional external clock enable signal to control the counter’ s count rate
- Upon clock timeout the WDT can perform the following tasks:
  - Generate a system reset signal
  - First generate an interrupt, even if the bit has been cleared by the interrupt service, and subsequently it will generate a system reset signal.
- Configurable duty cycle
- Programmable or hardware set counter start value
- Counter reset protection
- Pause mode, when the external pause signal is enabled
- WDT accidental disable protection
- Test mode for counter function test (decrement operation)
- External asynchronous clock support. When this function is enabled, a clock interrupt and a system reset signal will be generated even if the APB bus clock is off.

3.14 General Purpose Input/Output Interface (GPIO)

3.14.1 High speed GPIO

There are a total of 32 high-speed GPIO (GPIOHS). They have the following characteristics:

- Configurable as input or output
- Each IO is an independent interrupt source
- Edge-triggered or level-triggered interrupt support
- Each IO can be assigned to one of the 48 pins on the FPIOA
- Configurable pull-up and pull-down resistors, or high impedance mode

3.14.2 General purpose GPIO

There are 8 general-purpose GPIOs with the following characteristics:

- All 8 IOs are one interrupt source
- Configurable as input or output
- Edge-triggered or level-triggered interrupt support
- Each IO can be assigned to one of the 48 pins on the FPIOA
- Configurable pull-up and pull-down resistors, or high impedance mode

3.15 Direct Memory Access Controller (DMAC)

The DMAC is highly configurable, highly programmable, and highly efficient at transferring data in bus mode. The DMAC controller supports multi-master and multi-channel. DMAC has the following features:

- Memory-memory, memory-peripheral, peripheral-memory or peripheral-peripheral transfers
- Independent core and slave clocks
- The main interface can turn off its clock to save power when all peripherals are inactive
- Up to eight channels, each with their own source and destination pair
- Each channel data can only transmit in one direction at a time
- Input pin can dynamically select the destination size

- Channel lock support, support for internal channel arbitration, sets the privilege values of the main interface bus based on the priority of data transfer
- DMAC status output, idle/busy indication
- Each DMA transfer has interrupted, transmission completed, etc. status

3.16 Inter-Integrated Circuit Bus (I²C)

There are three I²C bus interfaces, each configurable as master or slave by the user.

- Standard mode (0 to 100Kb/s)
- Fast mode (<= 400Kb/s)
- 7-bit/10-bit addressing mode
- Bulk transfer mode
- Interrupt or polling mode operation

3.17 Serial Peripheral Interface (SPI)

There are four SPI interfaces; of which SPI0, SPI1 and SPI3 only support MASTER mode, and SPI2 only supports SLAVE mode.

- Support for 1/2/4/8 wire full duplex mode
- SPI0, SPI1, and SPI2 support up to 25MHz clock (TBC)
- SPI3 supports up to 100MHz clock (TBC)
- 32-bit wide, 32-byte deep FIFO
- Independently Masked Interrupts: host conflict, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, receive FIFO overflow
- Support for DMA transfers
- Support for dual-edge DDR transmission mode
- SPI3 supports XIP

3.18 Inter-Integrated Sound (I²S)

There are 3 I²S interfaces on board (I2S0, I2S1 and I2S20, all of which only support MASTER mode. I2S0 can be connected to the voice processing module to enable voice enhancement and sound source orientation. All interfaces support the follow-

ing other features:

- 8-bit, 16-bit or 32-bit configurable bus width
- Up to 4 stereo channels per interface
- Supports full-duplex communication, independent transmitter and receiver
- APB bus clock and I²S SCLK are asynchronous
- 12-bit, 16-bit, 20-bit, 24-bit or 32-bit audio data resolution
- I²S0 has a 64-byte deep transmit FIFO and 8-byte deep receive FIFO. Other interfaces have 8-byte deep transmit and receive FIFOs
- Support for DMA transfers
- Programmable FIFO threshold

3.19 TIMER

The system has three TIMER modules with the following characteristics:

- 32-bit counter width
- Configurable as up or down counter
- Independent clocks
- Configurable polarity for each interrupt
- Configurable individual or combined interrupt output flags
- Each timer has a read/write consistent register
- Timer reload output, switches whenever the timer counter is reloaded
- Output PWM mode, 0 %-100% duty cycle

3.20 Read Only Memory (ROM)

The AXI ROM is responsible for copying the user' s application program from SPI FLASH to the SRAM of the chip.

- Support for AES-128-CBC firmware decryption
- UOP mode to program FLASH
- SHA256 firmware integrity check for tamper resistance
- OTP configurable to disable UOP mode, SHA256 check, and AES decryption
- Support for entering TURBO mode, which enables the chip and its peripherals to run at higher frequencies during startup

3.21 Real Time Clock (RTC)

The RTC is a module for keeping track of real time, with the following characteristics:

- Support for external high frequency crystal reference
- Configurable external crystal frequency and frequency division ratio
- Configurable perpetual calendar, configurable items including century, year, month, day, hour, minute, second and week
- Can count in seconds and query current time
- Supports setting a set of alarms. The configurable items include year, month, day, hour, minute, and second. When the alarm arrives, the interrupt is triggered.
- Interrupt configurable to support daily, hourly, minute, and second trigger interrupts
- Readout counter count resolution less than 1 second, the resolution is one period of the external crystal oscillator
- Data cleared after power-on/reset

3.22 Pulse Width Modulation (PWM)

The PWM module is used to control the duty cycle of an external pulse output.
The user can configure the following functions of the PWM timer module:

- Frequency of pulses, by specifying the PWM timer frequency or period
- PWM timers can be configured to synchronize with other PWM timers or modules
- PWM timers can be in phase with other PWM timers or modules
- Timer count mode: up, down, or up and down in a loop
- Use the prescaler to change the rate of the PWM timer clock (PT_clk). Each timer has its own prescaler, configured by PWM_TIMERx_PRESCALE in the register PWM_TIMER0_CFG0_REG. The PWM timer is incremented or decremented at a slower rate depending on the setting of this register.

Chapter 4

Electrical Characteristics

Parameter	Name	Min	Typ	Max	Unit
3.3V/1.8V IO supply voltage	VDD	-	$3.3/1.8$	-	V
1.8V Digital supply voltage	$DVDD_{1.8V}$	-	1.8	-	V
1.8V Analog supply voltage	$AVDD_{1.8V}$	-	1.8	-	V
0.9V Core supply voltage	$VDD_{0.9V}$	-	0.9	-	V
3.3V IO supply current	$I_{3.3V}$	1	-	-	mA
1.8V Digital supply current	$I_{1.8V}$	1	-	-	mA
1.8V Analog supply current	$I_{1.8V}$	2	-	-	mA
0.9V Core supply current	$I_{0.9V}$	30	-	-	mA
3.3V/1.8V IO input high level	V_{IH}	$0.7 * VDD$	-	-	V
3.3V/1.8V IO input low level	V_{IL}	-	-	$0.3 * VDD$	V
IO High output level	V_{OH}	-	$VDD - 0.3$	-	mV
IO Low output level	V_{OL}	-	0.3	-	mV
IO Input leakage current	I_{IL}	-	**TBD**[*1]	-	nA
IO Input capacitance	C_{PAD}	-	**TBD**	-	pF
Storage Temperature	T_{STR}	-40	25	150	$°C$
Operating Temperature	T_{OPR}	-40	25	125	$°C$

4.1 Programmable Drive Capability

Low Level Output Current

[*1] Testing of this data is still in progress, and will be published in a future version of this document

DS[3:0]	Min(mA)	Typ(mA)	Max(mA)
0000	3.2	5.4	8.3
0001	4.7	8.0	12.3
0010	6.3	10.7	16.4
0011	7.8	13.2	20.2
0100	9.4	15.9	24.2
0101	10.9	18.4	28.1
0110	12.4	20.9	31.8
0111	13.9	23.4	35.5

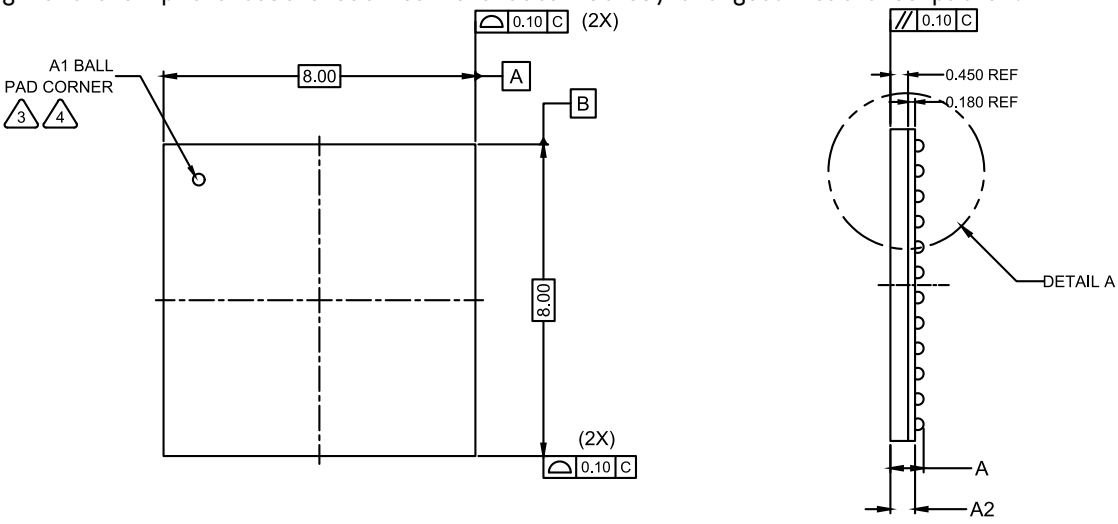
High Level Output Current

DS[3:0]	Min(mA)	Typ(mA)	Max(mA)
0000	5.0	7.6	11.2
0001	7.5	11.4	16.8
0010	10.0	15.2	22.3
0011	12.4	18.9	27.8
0100	14.9	22.6	33.3
0101	17.4	26.3	38.7
0110	19.8	30.0	44.1
0111	22.3	33.7	49.5

Chapter 5

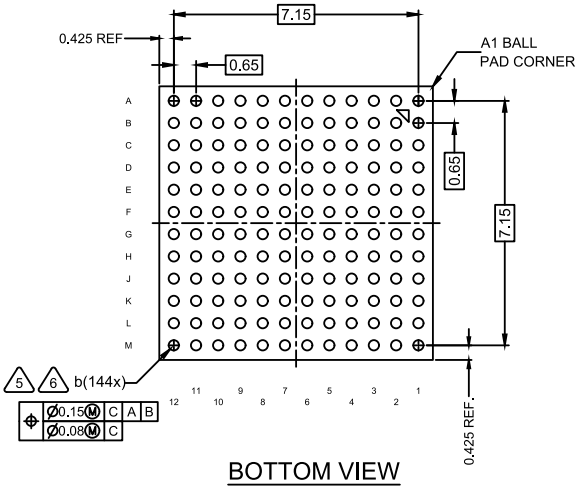
Package information

The chip is packaged in BGA144 with 12 balls on each side. The chip size is $8x8x0.953mm$ (BGA144C65P12X12_800X800X95). The package uses flip chip technology to give the chip the best electrical characteristics, and good heat dissipation.

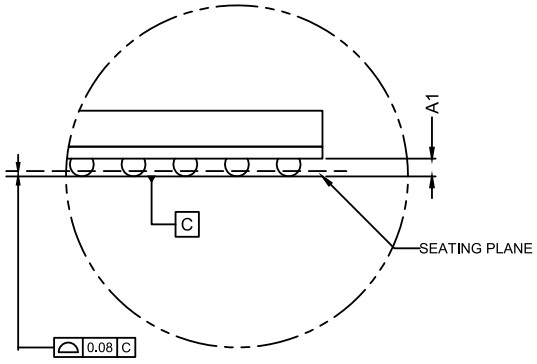


TOP VIEW

SIDE VIEW



BOTTOM VIEW



DETAIL A
ROTATED 90°

DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.753	0.853	0.953
A1	0.163	0.223	0.283
A2	0.550	0.630	0.710
b	0.250	0.300	0.350
NUMBER OF BALL 144			

UNLESS OTHERWISE SPECIFIED,
DIMENSIONS ARE IN MILIMETERS.

TOLERANCES ARE:		PACKAGE OUTLINE DRAWING
DECIMALS X.X ±0.1 X.XX ±0.05 X.XXX ±0.050	ANGLES ±1°	fcVFBGA 8.00mm X 8.00mm, 0.65mm PITCH, 144LD